CLAIMS

What is claimed is:

1. A method of forming a vertical PNP bipolar transistor in a BiCMOS process, where the transistor is formed upon a wafer having a silicon substrate, the method comprising:

forming a double diffused DWELL in a DNWELL formed within a P-epi layer formed across the substrate;

forming a SPWELL in the DNWELL region adjacent the DWELL region;

forming a layer of oxide material over the wafer, at least portions of the oxide layer forming gate oxide regions for MOS transistor devices on the wafer;

patterning the layer of oxide material to form an opening overlying and exposing silicon in a portion of the double diffused DWELL;

forming a layer of poly-silicon across the wafer;

patterning the layer of poly-silicon forming gate electrodes over the gate oxide regions for the MOS transistor devices and forming an emitter contact that fills the opening overlying the double diffused DWELL for the vertical PNP transistor; and

performing PSD/NSD implants to establish a collector contact and a base contact, respectively, for the vertical PNP transistor.

2. The method of claim1, wherein forming the DWELL comprises:

implanting a P-type dopant into the DNWELL through an opening in a mask to form a P-type body layer; and

implanting an N-type dopant into the P-type body layer through the same opening in the same mask to establish an N-type surface layer.

3. The method of claim 2, wherein the patterned poly-silicon comprises a P-type dopant that diffuses through the gate oxide opening into a small portion of the N-type surface layer of the DWELL, thereby establishing an emitter for the vertical PNP transistor.

4. The method of claim 3, wherein the emitter is about 0.8 by 0.8 microns in size.

5. The method of claim 1, wherein the PSD implant occurs within the SPWELL.

6. The method of claim 1, wherein the NSD implant occurs within the DWELL.

7. The method of claim 2, wherein the N-type surface layer serves as a base of the transistor.

8. The method of claim 2, wherein the P-type body layer serves as a collector of the transistor.

9. The method of claim 7, wherein the base has a thickness of about 0.2 to 0.5 microns.

10. The method of claim 2, wherein the DWELL is implanted with Boron at a concentration of $2e^{13}/cm^3$ at an energy level of 50 KeV, and then at a concentration of $1.5e^{14}/cm^3$ at an energy level of 400 KeV in forming the P-type body layer.

11. The method of claim 2, wherein the P-type body layer is implanted with Arsenic at a concentration of $7.5e^{13}/cm^3$ at an energy level of 160 KeV in forming the N-type surface layer.

12. The method of claim 1, further comprising:

forming an N buried layer (NBL) within the substrate so as to underlie the DNWELL and P-epi layer.

13. The method of claim 12, wherein the NBL comprises at least one of Arsenic and/or Antimony.

14. The method of claim 12, wherein forming the NBL comprises:

implanting a dopant of Antimony at a concentration of about $4.5e^{15}/cm^3$ at an energy level of about 60 KeV.

15. The method of claim 1, further comprising:

forming deep N+ regions within the P-epi layer adjacent the DNWELL.

16. The method of claim 3, wherein the patterned poly-silicon comprises Boron that diffuses into the N-type surface layer to establish an emitter for transistor.

17. The method of claim 1, wherein the DNWELL is implanted with a dopant of Boron at a concentration of about $1.6e^{13}/cm^3$ at an energy level of about 500KeV in forming the SPWELL.

18. A vertical PNP bipolar transistor formed as part of a BiCMOS process, the transistor formed upon a wafer having a silicon substrate and comprising:

a double diffused DWELL in a DNWELL formed within a P-epi layer formed across a substrate;

a SPWELL in the DNWELL region formed adjacent the DWELL region;

a layer of oxide material formed over the wafer and patterned so as to serve as a gate oxide in a CMOS/DMOS device;

a layer of poly-silicon formed across the wafer and patterned so as to serve as part of a gate stack in a CMOS/DMOS device, the patterned poly-silicon serving as an emitter contact for the vertical PNP transistor, the patterned poly-

silicon also comprising a P-type dopant that diffuses into a small portion of the DWELL, thereby establishing an emitter in the transistor; and

PSD/NSD implants that establish a collector contact and a base contact, respectively, for the vertical PNP transistor.

19. The transistor of claim 18, wherein the DWELL comprises:

a P-type body layer formed by a P-type dopant implanted into the DNWELL through an opening in a mask, the P-type body layer serving as a collector of the transistor; and

an N-type surface layer formed by an N-type dopant implanted into the P-type body layer through the same opening in the same mask, the N-type surface layer serving as a base of the transistor.

20. The transistor of claim 19, wherein at least one of the emitter is about 0.8 by 0.8 microns in size and the base has a thickness of about 0.2 to 0.5 microns.

21. A method of forming a transistor, comprising:

forming a well of a first conductivity type in a semiconductor body of a second conductivity type;

forming a mask over the semiconductor body with an opening overlying the well;

forming a collector region of the second conductivity type in the well using the mask;

forming a base region of the first conductivity type in the collector region using the mask;

forming an insulating layer over the semiconductor body;

forming an opening in the insulating layer over the base region;

forming a polysilicon layer doped with the second conductivity type over the insulating layer, the polysilicon layer filling the opening and contacting a portion of the base region associated with the opening; and

diffusing dopant of the second conductivity type into a top portion of the base region, wherein the top portion comprises an emitter region of the second conductivity type.

22. The method of claim 21, wherein the first conductivity type comprises n-type and the second conductivity type comprises p-type.

23. The method of claim 21, wherein forming the insulating layer comprises forming an oxide layer employed as a gate oxide layer for MOS type devices elsewhere in the semiconductor body.

24. The method of claim 23, wherein the polysilicon layer is employed as a gate electrode for the MOS type devices.

25. The method of claim 21, wherein the semiconductor body comprises an epitaxial layer formed over a semiconductor substrate.

26. The method of claim 25, wherein the well comprises a deep n-type well formed within the epitaxial layer.

27. The method of claim 26, wherein forming the collector region comprises:

performing a first implantation into the well through the mask opening with a p-type dopant having a first concentration and a first energy; and

performing a second implantation into the well with the p-type dopant having a second concentration and a second energy, wherein the first concentration is less than the second concentration and the first energy is less than the second energy.

28 The method of claim 27, wherein the p-type dopant comprises Boron, the first concentration is about $2e^{13}/cm^3$, and first energy is about 50 keV,

the second concentration is about $1.5e^{14}/cm^3$, and the second energy is about 400 keV.

29. The method of claim 27, wherein forming the base region comprises performing an n-type implant into the collector region through the mask opening, wherein a depth of the base region is less than a depth of the collector region.

30. The method of claim 29, wherein the n-type dopant comprises Arsenic, the concentration is about $7.5e^{13}/cm^3$, and the energy is about 160 keV.

31. The method of claim 21, further comprising forming a supplemental collector region within the well, the supplemental collector region laterally connecting to the collector region.

32. The method of claim 31, further comprising forming a collector contact region in the supplemental collector region, and a base contact region in the base region.

33. The method of claim 21, wherein the collector contact region and base contact region are formed using source/drain implants employed for MOS transistors elsewhere in the semiconductor body.